REMARKS

The present Amendment amends claims 1-8 and 17, and cancels claims 9-16 and 18-21. Therefore, the present application has pending claims 1-8 and 17.

35 U.S.C. §112 Rejections

Claims 17-21 stand rejected under 35 U.S.C. §112, second paragraph as allegedly failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. As previously indicated, claims 18-21 were canceled. Therefore this rejection regarding claims 18-21 is rendered moot.

This rejection regarding the remaining claim 17 is traversed for the following reasons. Contrary to the Examiner's assertions, Applicants submit that claim 17 is in compliance with the provisions of 35 U.S.C. §112. The Examiner alleges that claim 17 is indefinite because "The term "substantially" is not defined by the claim, and the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention" (citing MPEP §2173.05(b) and *In re Nehrenberg*, 280 F.2d 161, 126 USPQ 383 (CCPA 1960)).

However, as indicated in MPEP §2173.05(b), a claim ***may*** be rendered indefinite by reference to an object that is variable. Accordingly, the determination of whether a claim is rendered indefinite based on the use of the term "substantially" is fact specific. Applicants submit that the use of the term "substantially", in the manner claimed, distinguishes over the use of "substantially" as in the *Nehrenberg* case, and is analogous to the use of "substantially" as in *Andrew Corp. v. Gabriel Electronics*, 847 F.2d 819, 6 USPQ2d 2010 (Fed. Cir. 1988), which is also cited in MPEP §2173.05(b).

In *Andrew Corp.*, the court held that the limitation "which produces substantially equal E and H plane illumination patterns" was definite because one of ordinary skill in the art would know what was meant by "substantially equal." Likewise, in the present invention, Applicants submit that the limitation "wherein each of numbers of instructions of the mutually concurrently executable program blocks to be assigned to each of the processors are made substantially equal" is definite because one of ordinary skill in the art would know what was meant by "substantially equal" in the manner claimed.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of claim 17 under 35 U.S.C. §112, second paragraph.

35 U.S.C. §101 Rejections

Claims 15, 16 and 21 stand rejected under 35 U.S.C. §101 as allegedly being directed to non-statutory subject matter. As previously indicated, claims 15, 16 and 21 were canceled. Therefore, this rejection regarding claims 15, 16 and 21 is rendered moot.

35 U.S.C. §103 Rejections

Claims 1, 3-7 and 9-21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,370,560 to Robertazzi et al. ("Robertazzi") in view of U.S. Patent No. 5,978,831 to Ahamed et al. ("Ahamed"). As previously indicated, claims 9-16 and 18-21 were canceled. Therefore, this rejection regarding claims 9-16 and 18-21 is rendered moot. This rejection regarding the remaining claims 1, 3-7 and 17 is traversed for the following reasons. Applicants submit that the features of the present invention, as now more clearly recited in claims 1, 3-7 and 17, are not taught or suggested by Roberazzi or Ahamed, whether taken individually or in combination with each other in the manner suggested by the

Examiner. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw this rejection.

Amendments were made to the claims to more clearly describe features of the present invention. Specifically, amendments were made to the claims to more clearly recite that the present invention is directed to a decentralized control system as recited, for example, in independent claim 1.

The present invention, as recited in claim 1, provides a decentralized control system. The control system includes a plurality of processors; a plurality of devices controlled by the plurality of processors; and at least one information transmission path for communicating control information between the plurality of processors and for communicating input/output information between the plurality of processors and the devices.

According to the present invention, each of the plurality of processors includes a processor detecting means. The processor detecting means detects a connection state of each of the plurality of processors with respect to the information transmission path, where the connection state shows which processors of the plurality of processors are connected for controlling the plurality of devices, and is represented by an ID of each of the processors.

Also according to the present invention, the processor detecting means generates a list of available processors. At least one of the plurality of processors includes a program block assigning means and a program storage means. The program block assigning means assigns, based on the detected connection state detected by the processor detecting means, a plurality of mutually concurrently executable program blocks to control the device to each of the plurality of processors, respectively. The assigning means divides a program for controlling the

devices into the mutually concurrently executable plurality of blocks allowing uniform assignment of a processing load to the processors in accordance with an average number of execution steps or an average processing time for one cycle of each of the plurality of program blocks. The assigning means also generates an assignment list, and distributes the assignment list and the mutually concurrently executable plurality of blocks to the processors.

The program storage means stores a relevant one of the plurality of mutually concurrently executable program blocks at each of the plurality of processors, where each of the plurality of processors executes the stored relevant program blocks, respectively. According to the present invention, each of the plurality of processors distributes the mutually concurrently executable plurality of blocks and the assignment list, and executes the program blocks based on the assignment list. The prior art does not teach or suggest all of these features.

The above described features of the present invention, as now more clearly recited in the claims, are not taught or suggested by any of the references of record. Specifically, the features are not taught or suggested by either Robertazzi or Ahamed, whether taken individually or in combination with each other.

Robertazzi teaches a load sharing controller for optimizing resource utilization cost. However, there is no teaching or suggestion in Robertazzi of the decentralized control system as recited in claim 1 of the present invention.

Robertazzi discloses a load sharing system which minimizes overall costs by assigning segments of a divisible load to distributed processor platforms based on the resource utilization cost of each processor platform. The distributed processor platforms are connected via data links which also have associated resource utilization costs. A controller divides a divisible load or task and assigns each

segment of the load or task to a processor platform based on the processor platform's resource utilization cost and data link cost. After the initial allocation, an optimizing reallocation is performed to reduce the overall monetary cost processing the load or task. The optimization can be performed using a pair-wise swapping technique.

One feature of the present invention, as recited in claim 1, includes where the program block assigning means assigns, based on the detected connection state detected by the processor detecting means, a plurality of mutually concurrently executable program blocks to control the device to each of the plurality of processors, respectively. Robertazzi does not disclose this feature.

In the present invention, a system obtains the status of each of the processors to determine by a particular selected one of the processors, how each of a plurality of programs to be performed are distributed to each of the processors, and to totally control each of such programs to be performed in the entire system. In such a system, it is possible to automatically determine the distribution of programs in accordance with the status of a controlling processor.

As described in column 6, lines 37-65, and as shown in Fig. 1C, Robertazzi teaches a data file 150, which includes a cost column 187 and a speed column 185. The cost column 187 indicates the relative monetary cost of the processor platform, and the speed column 185 indicates the relative speed of the processor platform. As specifically described in lines 50-51 of column 6, the cost column and the speed column's coefficient are used to generate a cost/unit task-load. As described in column 8, lines 34-35, the cheapest available participating processor platform is based on the cost/unit task-load. This is quite different from the present invention, where the plurality of mutually concurrently executable program blocks to control is

assigned based on the detected connection state detected by the processor detecting means. Accordingly, the present invention distinguishes from Robertazzi.

Another feature of the present invention, as recited in claim 1, includes wherein the program block assigning means divides a program for controlling the devices into the mutually concurrently executable plurality of blocks allowing uniform assignment of a processing load to the processors in accordance with an average number of execution steps or an average processing time for one cycle of each of the plurality of program blocks, generates an assignment list, and distributes the assignment list and the mutually concurrently executable plurality of blocks to the processors. Robertazzi does not disclose this feature.

For example, Robertazzi does not teach or suggest where the assigning means generates an assignment list and distributes the assignment list and the mutually concurrently executable plurality of blocks to the processors, as in the present invention. In Robertazzi, a system is arranged to only distribute loads to each of the processors. That is to say, each of the processors in Robertazzi's system is not arranged to actively operate in order to perform distributed programs according to a share list for programs having also been distributed, as in the present invention.

Yet another feature of the present invention, as recited in claim 1, includes where each of the plurality of processors distributes the mutually concurrently executable plurality of blocks and the assignment list, and executes the program blocks based on the assignment list. Robertazzi does not disclose this feature.

As previously discussed, Robertazzi's system is arranged to only distribute loads to each of the processors. That is to say, each of the processors in Robertazzi's system is not arranged to actively operate in order to perform

distributed programs according to a share list for programs having also been distributed, as in the present invention.

Therefore, Robertazzi fails to teach or suggest "program block assigning means for assigning, based on the detected connection state detected by said processor detecting means, a plurality of mutually concurrently executable program blocks to control the device to each of said plurality of processors, respectively" as recited in claim 1.

Furthemore, Robertazzi fails to teach or suggest "wherein said program block assigning means divides a program for controlling said devices into said mutually concurrently executable plurality of blocks allowing uniform assignment of a processing load to the processors in accordance with an average number of execution steps or an average processing time for one cycle of each of the plurality of program blocks, said generates an assignment list, and distributes the assignment list and said mutually concurrently executable plurality of blocks to said processors" as recited in claim 1.

Further, Robertazzi fails to teach or suggest "wherein each of said plurality of processors distributes said mutually concurrently executable plurality of blocks and said assignment list, and executes the program blocks based on said assignment list" as recited in claim 1.

The above noted deficiencies of Robertazzi are not supplied by any of the other references of record, namely Ahamed, whether taken individually or in combination with each other. Therefore, combining the teachings of Robertazzi and Ahamed in the manner suggested by the Examiner still fails to teach or suggest the features of the present invention as now more clearly recited in the claims.

Ahamed teaches a synchronous multiprocessor that uses tasks, which are directly proportional in size to the individual processors rates. However, there is no teaching or suggestion in Ahamed of the decentralized control system as recited in claim 1 of the present invention.

Ahamed discloses a game hoist for mounting to the cargo rack of an all-terrain vehicle (ATV). The game hoist is mounted to the cargo rack using a base plate which has one or more sets of angle brackets mounted to the underside of the base plate. The sets of angle brackets form pockets or receptacles to slidably receive respective rods of the cargo rack. The base plate has an upward facing cylindrical post which receives a cylindrical column. A telescoping boom is provided with a cylindrical collar which fits over the top end of the column. The telescoping boom has an inner cylindrical member which is slidingly received in an outer cylindrical member. The inner cylindrical member may be telescoped outward from the outer cylindrical member. The outer end of the inner cylindrical member is provided with a manually operated winch. The winch is desirably provided with a ratchet mechanism.

One feature of the present invention, as recited in claim 1, includes where the program block assigning means assigns, based on the detected connection state detected by the processor detecting means, a plurality of mutually concurrently executable program blocks to control the device to each of the plurality of processors, respectively. Ahamed does not disclose this feature, and the Examiner does not rely upon Ahamed for teaching this feature.

Another feature of the present invention, as recited in claim 1, includes wherein the program block assigning means divides a program for controlling the devices into the mutually concurrently executable plurality of blocks allowing uniform

assignment of a processing load to the processors in accordance with an average number of execution steps or an average processing time for one cycle of each of the plurality of program blocks, the generates an assignment list, and distributes the assignment list and the mutually concurrently executable plurality of blocks to the processors. Ahamed does not disclose this feature.

For example, Ahamed does not teach or suggest where the assigning means generates an assignment list and distributes the assignment list and the mutually concurrently executable plurality of blocks to the processors, as in the present invention. More specifically, there is no teaching or suggestion in Ahamed of where an assignment list is distributed, and where a processor that has received the list performs the programs.

Yet another feature of the present invention, as recited in claim 1, includes where each of the plurality of processors distributes the mutually concurrently executable plurality of blocks and the assignment list, and executes the program blocks based on the assignment list. Ahamed does not disclose this feature. As previously discussed, for example, there is no teaching or suggestion in Ahamed of where an assignment list is distributed, and where a processor that has received the list performs the programs.

Therefore, Ahamed fails to teach or suggest "program block assigning means for assigning, based on the detected connection state detected by said processor detecting means, a plurality of mutually concurrently executable program blocks to control the device to each of said plurality of processors, respectively" as recited in claim 1.

Furthermore, Ahamed fails to teach or suggest "wherein said program block assigning means divides a program for controlling said devices into said mutually

concurrently executable plurality of blocks allowing uniform assignment of a processing load to the processors in accordance with an average number of execution steps or an average processing time for one cycle of each of the plurality of program blocks, said generates an assignment list, and distributes the assignment list and said mutually concurrently executable plurality of blocks to said processors" as recited in claim 1.

Further, Ahamed fails to teach or suggest "wherein each of said plurality of processors distributes said mutually concurrently executable plurality of blocks and said assignment list, and executes the program blocks based on said assignment list" as recited in claim 1.

Both Robertazzi and Ahamed suffer from the same deficiencies, relative to the features of the present invention, as recited in the claims. Therefore, combining the teachings of Robertazzi and Ahamed in the manner suggested by the Examiner does not render obvious the features of the present invention as now more clearly recited in the claims. Accordingly, reconsideration and withdrawal of the 35 U.S.C. §103(a) rejection of claims 1, 3-7 and 17 as being unpatentable over Robertazzi in view of Ahamed are respectfully requested.

Claims 2 and 8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Robertazzi in view of Ahamed, and further in view of U.S. Patent No. 5,592,671 to Hirayama. Claims 2 and 8 are dependent on claim 1. Therefore, claims 2 and 8 are allowable for at least the same reasons previously discussed regarding independent claim 1.

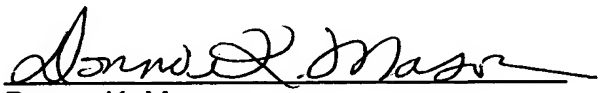
The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the references used in the rejection of claims 1-8 and 17.

In view of the foregoing amendments and remarks, Applicants submit that claims 1-8 and 17 are in condition for allowance. Accordingly, early allowance of claims 1-8 and 17 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C., Deposit Account No. 50-1417 (referencing Attorney Docket No. 500.37600CX1).

Respectfully submitted,

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.



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